Our Docket No.: 51876P451
Express Mail No.: EV339912942US

UTILITY APPLICATION FOR UNITED STATES PATENT

FOR

METHOD FOR FORMING FLOWABLE DIELECTRIC LAYER IN SEMICONDUCTOR DEVICE

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METHOD FOR FORMING FLOWABLE DIELECTRIC LAYER IN SEMICONDUCTOR DEVICE

Field of the Invention

The present invention relates to a method for manufacturing a semiconductor device; and, more particularly, to a method for forming a flowable dielectric layer by employing a barrier layer on sidewalls of the patterned flowable dielectrics.

Description of the Prior Art

In recent years, as a semiconductor technology advances, circuit elements and interconnections on a wafer or a semiconductor substrate become increasingly denser and denser. In order to prevent unwanted interactions between these circuit elements, insulator-filled gaps or trenches located therebetween are provided to physically and electrically isolate the elements and conductive lines. However, as circuit densities continue to increase, the widths of these gaps decrease, thereby increasing gap aspect ratios which are typically defined as the gap height divided by the gap width. As a result, it is very difficult to fill these narrow and deep gaps with a predetermined gap-fill material, which can lead to unwanted voids and discontinuities in an insulating layer. Therefore, in attempt to address this problem, there

have been proposed techniques for forming the insulating layer by using a material such as a borophosphosilicate glass (BPSG), a high density plasma (HDP) oxide or the like, for improving a gap-fill property of the insulating layer.

In general, in case of employing the BPSG as an insulating material, it shows a good gap-fill property but still a drawback that there may be happened the diffusion phenomenon of the dopant in a transistor during a high thermal process, i.e., a reflow process.

Meanwhile, an HDP process is recently used to fill high aspect ratio gaps. Typical HDP process employs a chemical vapor deposition (CVD) with a gas mixture containing oxygen, silane, and inert gases such as argon, to achieve a simultaneous dielectric etching and deposition. In the HDP process, an RF bias is applied to a wafer substrate in a reaction chamber. Some of these gas molecules, i.e., particularly argon, are ionized in the plasma and accelerate toward the wafer surface when the RF bias is applied to the wafer. Material is thereby sputtered when ions strike the surface. As a result, an insulating material deposited on the wafer surface is simultaneously sputter etched to help to keep the gaps open during the deposition process, which allows higher aspect ratio gaps to be filled. Although the HDP process has the aforementioned advantage for filling the high aspect ratio gaps, it suffers from shortcomings that there may be happened etch damages of an underlying layer due to a plasma and further, edges of a micro-pattern are eroded while

repeating the deposition and the sputter etch during the HDP process.

In attempt to overcome the above problems, therefore, there is proposed another technique utilizing a flowable dielectric for filling the narrow and the deep gaps, i.e., the high aspect ratio gaps, and for protecting the underlying layer from the damage in fabricating the semiconductor device.

Referring to Figs. 1A to 1D, there are shown cross sectional views setting forth a conventional method for forming a flowable dielectric layer 120 in a semiconductor device.

In Fig. 1A, a semiconductor substrate 110 where an active area 112 and a field area 114 are defined, is prepared in advance by a predetermined process. Thereafter, a plurality of gates 116 with narrow widths are formed on predetermined locations of a top face of the semiconductor substrate 110. Afterward, a predetermined insulating layer (not shown) is formed over the resultant structure and is anisotropically etched into a first predetermined configuration, thereby forming sidewall spacers 118 on the gates 116. Subsequently, a flowable dielectric layer 120 is formed over the resultant structure embracing the gates 116 and the sidewall spacers 118.

In an ensuing step, referring to Fig. 1B, an annealing process is carried out in a furnace for removing moisture existing in the flowable dielectric layer 120 and densifying the flowable dielectric layer 120. During the annealing

process, there is happened a chemical reaction in the flowable dielectric layer 120. That is, silane (SiH_4) and hydrogen peroxide (H_2O_2) are inter-reacted in the flowable dielectric layer 120, to thereby produce Si-O bonds and O-H bonds. Therefore, O-H bonds are again inter-reacted with each other to form a byproduct of water (H_2O) by means of a dehydration reaction. The water produced during the dehydration reaction is removed during the annealing process so that there are formed a plurality of micro-pores 115 in the flowable dielectric layer 120. In particular, a top face of the flowable dielectric layer 120 is shrunk to condense the flowable dielectric layer 120 so that the micro-pores 115 are rarely formed in a top region thereof. However, since a bottom face of the flowable dielectric layer 120 is fixed to a wafer surface, a bottom region of the flowable dielectric layer 120 is hardly shrunk, whereby the micro-pores 115 are formed during the annealing process.

After carrying out the annealing process, the flowable dielectric layer 120 is planarized till top faces of the gates 116 are exposed by using a method such as a chemical mechanical polishing (CMP).

In a next step, referring to Fig. 1C, contact masks (not shown) are formed on predetermined locations of the top face of the flowable dielectric layer 120. Afterward, the flowable dielectric layer 120 is patterned into a second predetermined configuration by using the contact masks as etch masks, thereby forming a plurality of contact holes 101 and patterned

flowable dielectrics 120A. In Fig. 1C, it is understood that the micro-pores 115 still remain in the patterned flowable dielectrics 120A.

In a subsequent step, a pre-cleaning process is carried out for removing a natural oxide (not shown) formed after the formation of the contact holes 101, thereby securing a bottom area of the contact holes 101. While the pre-cleaning process is performed, the micro-pores 115 are enlarged gradually. That is, the micro-pores 115 formed on the sidewalls of the patterned flowable dielectrics 120A are eroded gradually by a solution for use in the pre-cleaning process. As a result, enlarged micro-pores 115A are formed on the sidewalls of the patterned flowable dielectrics 120A, as shown in Fig. 1C.

Following the pre-cleaning process, referring to Fig. 1D, a polysilicon layer is formed over the resultant structure so that the contact holes 101 are filled with the polysilicon and then, is planarized by using a method such as the CMP or an etchback process, thereby forming contact plugs 121 and 122, wherein one contact plug 121 is disposed between the gates 116 and the other contact plugs 122 are disposed aside the patterned flowable dielectrics 120A. Since the micro-pores 115A became enlarged during the pre-cleaning process, the polysilicon encroaches into the enlarged micro-pores 115A formed on the sidewalls of the patterned flowable dielectrics 120A, thereby forming rugged sidewall surfaces 126 of the conductive plugs 122 which are disposed aside the patterned flowable dielectrics 120A.

Referring to Figs. 2A and 2B, there are shown micrographs of a scanning electron micrography (SEM) depicting the micro-pores 115 existing in the patterned flowable dielectrics 120A and the conductive plugs 122 having the rugged sidewall surfaces 126.

In Fig. 2A, it is understood that the micro-pores 115 are formed in the patterned flowable dielectric layer 120A except the top regions of the patterned flowable dielectrics 120A, after carrying out the annealing process. That is, since the bottom regions of the patterned flowable dielectrics 120A are rarely shrunk during the annealing process, there are inevitably formed micro-pores 115 in the middle and the bottom regions of the flowable dielectric layer 120.

Fig. 2B shows the micrograph that the polysilicon encroaches into the enlarged micro-pores 115A after carrying out the pre-cleaning process and the process for forming the polysilicon layer. As aforementioned, the micro-pores 115A formed during the annealing process are enlarged during the pre-cleaning process. Therefore, the conductive plugs 122 disposed aside the patterned flowable dielectrics 120A have the rugged sidewall surface 126 encroaching into the patterned flowable dielectrics 120A so that there may be generated a leakage current between adjacent contact plugs, i.e., the bridge phenomenon. Furthermore, as a modern semiconductor device is much more miniaturized, the polysilicon encroaching into the enlarged micro-pores 115A of the patterned flowable dielectrics 120A becomes a serious problem because the modern

semiconductor demands dense and miniaturized patterns. Thus, it is difficult to apply the conventional aforementioned process for forming the flowable dielectric layer to the miniaturized semiconductor device having the patterns of the high aspect ratio.

Summary of the Invention

It is, therefore, an object of the present invention to provide a method for forming a flowable dielectric layer in a semiconductor device by forming a barrier layer on sidewalls of a patterned flowable dielectric, thereby preventing contact plugs encroaching into micro-pores in the patterned flowable dielectric.

In accordance with one aspect of the present invention, there is provided a method for forming a flowable dielectric layer in a semiconductor device, the method including the steps of: a) forming a plurality of patterns on a semiconductor substrate, wherein narrow and deep gaps are formed therebetween; b) forming a flowable dielectric layer so as to fill the gaps between the patterns; c) carrying out an annealing process for densifying the flowable dielectric layer and removing moisture therein; d) forming a plurality of contact holes by selectively etching the flowable dielectric layer so as to expose predetermined portions of the semiconductor substrate; e) forming a barrier layer on sidewalls of the contact holes for preventing micro-pores in

the flowable dielectric layer; f) carrying out a cleaning process in order to remove native oxides and defects on the semiconductor substrate; and g) forming a plurality of contact plugs by filling a conductive material into the contact plugs.

Brief Description of the Drawings

The above and other objects and features of the present invention will become apparent from the following description of the preferred embodiments given in conjunction with the accompanying drawings, in which:

Figs. 1A to 1D are cross sectional views setting forth a conventional method for forming a flowable dielectric layer in a semiconductor device;

Figs. 2A and 2B are micrographs of a scanning electron micrography (SEM) depicting the micro-pores existing in the flowable dielectric layer and the conductive plugs encroaching into the micro-pores of the flowable dielectric layer according to the conventional method; and

Figs. 3A to 3F are cross sectional views setting forth a method for forming a flowable dielectric layer in a semiconductor device in accordance with a preferred embodiment of the present invention.

Detailed Description of the Preferred Embodiments

There are provided in Figs. 3A to 3F cross sectional

views setting forth a method for forming a flowable dielectric layer in a semiconductor device in accordance with a preferred embodiment of the present invention.

In Fig. 3A, an inventive method begins with preparing a semiconductor substrate 210 obtained where field oxide (FOX) areas 214 and an active area 212 are defined in preset locations of the semiconductor substrate 210 by a predetermined process. Thereafter, gates 216 are formed on predetermined locations of a top face of the semiconductor substrate 210, wherein there is formed a gap between adjacent gates 216 having a narrow space. Afterward, sidewall spacers 218 are formed on sidewalls of the gates 216 by using a typical etching process in which the sidewall spacers 218 uses a silicon nitride. As is well known, there are typically formed gate oxides (not shown) beneath the gates 216 and the gates 216 may be a stack structure of a polysilicon layer, a metal layer and a hard mask. Here, the metal layer and the hard mask use tungsten and nitride, respectively.

In a next step, a flowable dielectric layer 220 is formed over the resultant structure by using a spin on dielectric (SOD) such as a silicate, a siloxane, a methyl SilsesQuioxane (MSQ), a hydrogen SisesQuioxane(HSQ), an MSQ/HSQ, a perhydrosilazane (TCPS) or a polysilazane. Alternatively, the flowable dielectric layer 220 can be formed by using a low temperature undoped dielectric at a temperature in a range of about -10 _ to about 150 _ under a pressure ranging from about 10 mTorr to about 100 Torr, wherein a reaction source uses a

mixture gas of $SiH_x(CH_3)_y$ ($0 \leq x \leq 4$, $0 \leq y \leq 4$), H_2O_2, O_2, H_2O and N_2O. It is preferable that the thickness of the flowable dielectric layer 220 is in the range of about 1,000 _ to about 20,000 _ in consideration of heights of the gates 216 and a gap space between the gates 216.

After forming the flowable dielectric layer 220, referring to Fig. 3B, an annealing process is carried out in a furnace at a temperature ranging from about 300 _ to about 1,000 _, for densifying the flowable dielectric layer 220 and for removing moisture therein. During the annealing process, there are formed a plurality of micro-pores 215 in the flowable dielectric layer 220. In detail, during the annealing process, there is happened a chemical reaction in the flowable dielectric layer 220. That is, silane (SiH_4) and hydrogen peroxide (H_2O_2) are inter-reacted in the flowable dielectric layer 220, to thereby produce Si-O bonds and O-H bonds. Therefore, O-H bonds are again inter-reacted with each other to form a byproduct of water (H_2O) by means of a dehydration reaction. The water produced during the dehydration reaction is removed during the annealing process so that there are formed a plurality of micro-pores 215 in the flowable dielectric layer 220. In particular, a top face of the flowable dielectric layer 220 is shrunk to condense the flowable dielectric layer 120 so that the micro-pores 215 are rarely formed in a top region thereof. However, since a bottom face of the flowable dielectric layer 220 is fixed to a wafer surface, a bottom region of the flowable dielectric

layer 220 is hardly shrunk, whereby the micro-pores 215 are formed during the annealing process.

Afterward, the flowable dielectric layer 220 is planarized till the top faces of the gates 216 are exposed by using the CMP process. The reason of carrying out the planarization process before forming contact holes 201 is to secure a wider area in a bottom region of the contact holes 201 because an etch profile is slightly inclined toward the bottom faces of the contact holes 201.

Subsequently, referring to Fig. 3C, preset contact masks (not shown) are formed on predetermined locations of the top face of the planarized flowable dielectric layer 220. Afterward, the planarized flowable dielectric layer 220 is pattered into a predetermined configuration by using the preset contact masks so as to form the contact holes 201 and patterned flowable dielectrics 220A.

Following the formation of the contact holes 201, a pre-cleaning process is carried out for removing a native oxide and defects formed on the semiconductor substrate 210 by using a method such as a wet cleaning or a dry cleaning process. Therefore, it is possible to secure bottom areas of the contact holes 201 without the native oxide and the defects. Like the prior art, the micro-pores 215 on the sidewalls of the patterned flowable dielectrics 220A are gradually enlarged during the pre-cleaning process, thereby forming enlarged micro-pores 215A.

Thereafter, referring to Fig. 3D, a barrier layer 226 is

formed on bottom faces and sidewalls of the patterned flowable dielectrics 220A and the bottom faces of the contact holes 201 with a thickness in the range of about 20 _ to about 300 _ for preventing a gas or a solution infiltrating into the micro-pores in the patterned flowable dielectrics 220A. Herein, the barrier layer 226 uses a material such as a silicon nitride, a silicon oxide, a silicon carbide or the like.

After the formation of the barrier layer 226, referring to Fig. 3E, portions of the barrier layer 226 formed on the top faces of the patterned flowable dielectrics 220A and the bottom faces of the contact holes 201 are removed by using a dry etching process, e.g., a blanket etch process. Therefore, the barrier layer 216 exists only on the sidewalls of the patterned flowable dielectrics 220A. Thereafter, a post-cleaning process is carried out for removing another native oxide and defects formed on the semiconductor substrate 210 by using a method such as a wet cleaning or a dry cleaning process. In the present invention, there is introduced the barrier layer 226 before forming contact plugs 221 and 222, it is possible to prevent the micro-pores existing on the sidewalls of the patterned flowable dielectrics 220A being enlarged during the post-cleaning process. Accordingly, the polysilicon in the contact plugs 221 and 222 does not encroach into the enlarged micro-pores 115A of the patterned flowable dielectrics 220A so that a bridge between the adjacent contact plugs 221 and 222 can not be generated.

Afterward, referring to Fig. 3F, a conductive layer such

as the polysilicon is deposited over the resultant structure and is planarized by using a method such as the CMP process or an etchback process, thereby forming the contact plugs 221 and 222. Among the contact plugs 221 and 222, one of the contact plugs 222 serves as a storage node contact plug and the other contact plug 221 serves as a bit line contact.

As described above, in comparison with the prior art method, the barrier layer 226 is formed on the sidewalls of the patterned flowable dielectrics 220A before carrying out a post-cleaning process. Therefore, the polysilicon in the contact plugs 221 and 222 can not diffuse into the micro-pores in the patterned flowable dielectrics 220A. As a result, the bridge phenomenon between adjacent contact plugs 221 and 222, which is a serious problem in the prior art method, is effectively prevented.

Furthermore, the formation of the flowable dielectric layer 220 is carried out at a low temperature, thereby preventing the diffusion of the dopant in a transistor. Additionally, since the barrier layer 226 is employed before the process for forming contact plugs 221 and 222, it is possible to secure a cleaning process margin, to thereby enhance a contact resistance and remove defects existing in a wafer produced during the etch process easily.

While the present invention has been described with respect to the particular embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the scope of

the invention as defined in the following claims.